DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78081(A), 78082(A)

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78081(A) and 78082(A) are members of the μPD78083 Subseries of the 78K/0 Series microcontrollers. These products are produced with a more stringent quality assurance program than that of the μPD78081 and 78082 (standard models) (NEC classifies these products as "special products" by quality grade).

Besides a high-speed, high-performance CPU, these microcontrollers have on-chip ROM, RAM, I/O ports, 8-bit resolution A/D converter, timer, serial interface, interrupt control, and other peripheral hardware.

The μPD78P083(A) including a one-time PROM version which can operate in the same power supply voltage range as a mask ROM version, and various development tools are available.

The details of the functions are described in the following User's Manuals. Be sure to read the documents before starting design.

μPD78083 Subseries User's Manual : IEU-1407
78K/0 Series User's Manual Instructions : IEU-1372

FEATURES

- Internal ROM and RAM

Part Number \ Item	Program Memory (ROM)	Data Memory (Internal High-speed RAM)	Package
μPD78081(A)	8 Kbytes	256 bytes	44-pin plastic QFP (10 × 10 mm)
μPD78082(A)	16 Kbytes	384 bytes	

- Minimum instruction execution time can be changed from high-speed (0.4 μs) to low-speed (12.8 μs)
- I/O ports: 33
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 1 channel
  3-wire serial I/O/UART mode : 1 channel
- Timer : 3 channels
- Supply voltage : V_{DD} = 1.8 to 5.5 V

APPLICATION FIELDS

Controllers for automobile electronic control systems, gas detector circuit-breakers, various types of safety equipment, etc.

In addition to the μPD78081(A) and 78082(A), this Data Sheet also describes the μPD78081(A2). Unless otherwise specified, however, the μPD78081(A) and 78082(A) are used throughout this Data Sheet as the representative products, and their descriptions also apply to the μPD78081(A2).

Document No. U12436EJ1V0DS00 (1st edition)
Date Published July 1997 N
Printed in Japan

ORDERING INFORMATION

Part Number	Package
μPD78081GB(A)-×××-3B4	44-pin plastic QFP (10 × 10 mm)
μPD78081GB(A)-×××-3BS-MTX Note	44-pin plastic QFP (10 × 10 mm)
μPD78082GB(A)-×××-3B4	44-pin plastic QFP (10 × 10 mm)
μPD78082GB(A)-×××-3BS-MTX Note	44-pin plastic QFP (10 × 10 mm)
μPD78081GB(A2)-×××-3B4	44-pin plastic QFP (10 × 10 mm)

Note Under planning

Caution μPD78081GB(A) and 78082GB(A) have two kinds of package (Refer to 11. PACKAGE DRAWINGS). Please consult NEC's sales representative for the available package.

Remark ××× indicates ROM code suffix.

QUALITY GRADE

Special

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

DIFFERENCES BETWEEN μPD78081 AND 78082, AND μPD78081(A) AND 78082(A)

Item \ Part Number	μPD78081, 78082	μPD78081(A), 78082(A)
Quality grade	Standard	Special
Package	• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm)	44-pin plastic QFP (10 × 10 mm)

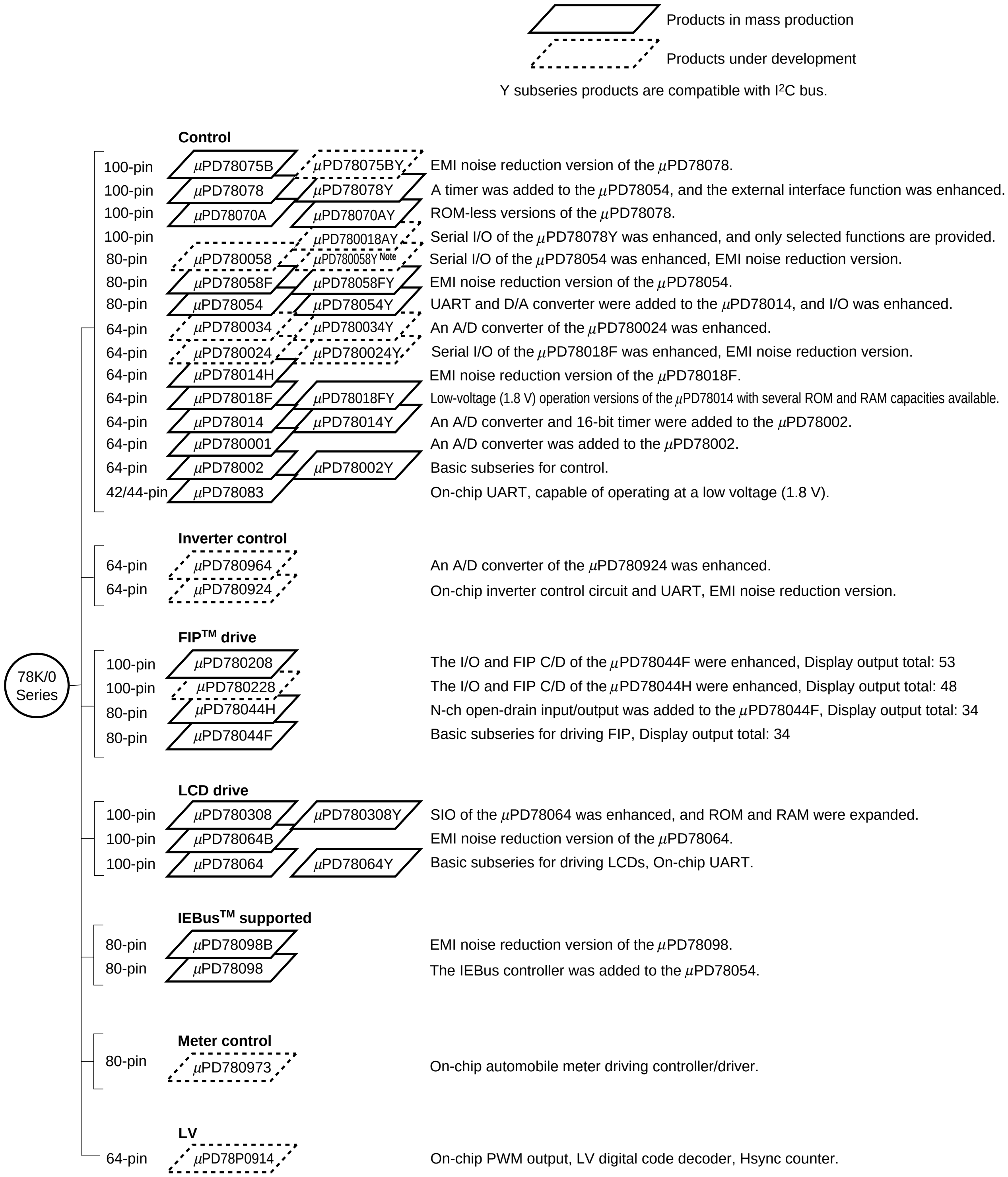
DIFFERENCES BETWEEN μPD78081(A) AND 78081(A2)

Item \ Part Number	μPD78081(A)	μPD78081(A2)
Supply voltage	V_{DD} = 1.8 to 5.5 V	V_{DD} = 5 V ±10%
Minimum instruction execution time	0.4 μs (at 5 MHz)	0.57 μs (at 7 MHz)
Operating ambient temperature	T_A = –40 to 85˚C	T_A = –40 to +125˚C

Remark In addition to the above parameters, the supply current also differs. For details, refer to **10. ELECTRICAL SPECIFICATIONS**.

78K/0 SERIES DEVELOPMENT

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.



Note Under planning

The following table shows the differences among subseries functions.

Subseries Name	Function	ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78075B	32 K to 40 K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	88	1.8 V	Available
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2ch						2ch	3ch (time-division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780034	8 K to 32 K					–	8ch	–	3ch (UART: 1ch, time-division 3-wire: 1ch)	51	1.8 V	
	μPD780024						8ch	–					
	μPD78014H									2ch	53		
	μPD78018F	8 K to 60 K											
	μPD78014	8 K to 32 K										2.7 V	
	μPD780001	8 K		–	–					1ch	39		–
	μPD78002	8 K to 16 K			1ch		–				53		Available
	μPD78083				–		8ch			1ch (UART: 1ch)	33	1.8 V	–
Inverter	μPD780964	8 K to 32 K	3ch	**Note**	–	1ch	–	8ch	–	2ch (UART: 2ch)	47	2.7 V	Available
control	μPD780924						8ch	–					
FIP	μPD780208	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
drive	μPD780228	48 K to 60 K	3ch	–	–					1ch	72	4.5 V	
	μPD78044H	32 K to 48 K	2ch	1ch	1ch						68	2.7 V	
	μPD78044F	16 K to 40 K								2ch			
LCD	μPD780308	48 K to 60 K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time-division UART: 1ch)	57	2.0 V	–
drive	μPD78064B	32 K								2ch (UART: 1ch)			
	μPD78064	16 K to 32 K											
IEBus	μPD78098B	40 K to 60 K	2ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	69	2.7 V	Available
supported	μPD78098	32 K to 60 K											
Meter control	μPD780973	24 K to 32 K	3ch	1ch	1ch	1ch	5ch	–	–	2ch (UART: 1ch)	56	4.5 V	–
LV	μPD78P0914	32 K	6ch	–	–	1ch	8ch	–	–	2ch	54	4.5 V	Available

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTION

Item		Part Number μPD78081(A)	μPD78082(A)
Internal memory	ROM	8 Kbytes	16 Kbytes
	Internal high-speed RAM	256 bytes	384 bytes
Memory space		64 Kbytes	
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		On-chip minimum instruction execution time selective function 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at main system clock of 5.0 MHz)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD adjustment, etc.	
I/O ports		Total : 33 • CMOS input : 1 • CMOS I/O : 32	
A/D converter		8-bit resolution × 8 channels	
Serial interface		3-wire serial I/O/UART mode selectable : 1 channel	
Timer		• 8-bit timer/event counter : 2 channels • Watchdog timer : 1 channel	
Timer output		2 (8-bit PWM output)	
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock of 5.0 MHz)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock of 5.0 MHz)	
Vectored interrupt sources	Maskable	Internal : 8, external : 3	
	Non-maskable	Internal : 1	
	Software	1	
Supply voltage		V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		44-pin plastic QFP (10 × 10 mm)	

Caution The supply voltage and other parameters of the μPD78081(A2) differ from those of the other models. For details, refer to "DIFFERENCES BETWEEN μPD78081(A) AND 78081(A2)".

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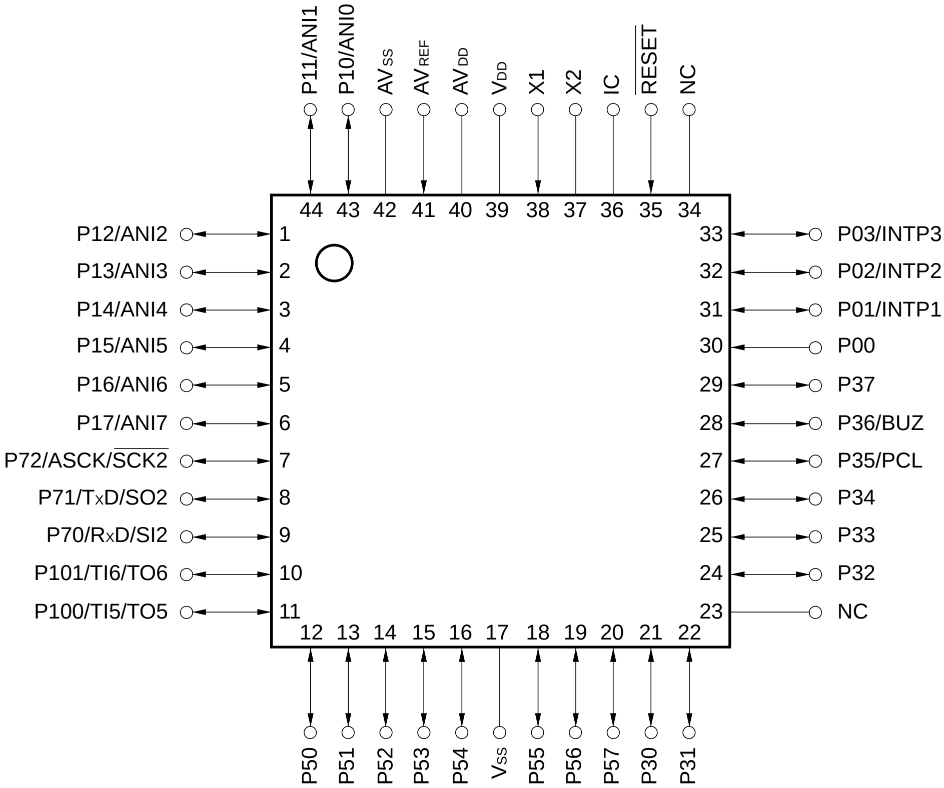
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1. PIN CONFIGURATION (Top View)

- **44-pin plastic QFP (10 × 10 mm)**
  μPD78081GB(A)-×××-3B4
  μPD78081GB(A)-×××-3BS-MTX **Note**
  μPD78082GB(A)-×××-3B4
  μPD78082GB(A)-×××-3BS-MTX **Note**
  μPD78081GB(A2)-×××-3B4



Note Under planning

Cautions 1. Connect IC (Internally Connected) pin directly to V_{SS}.

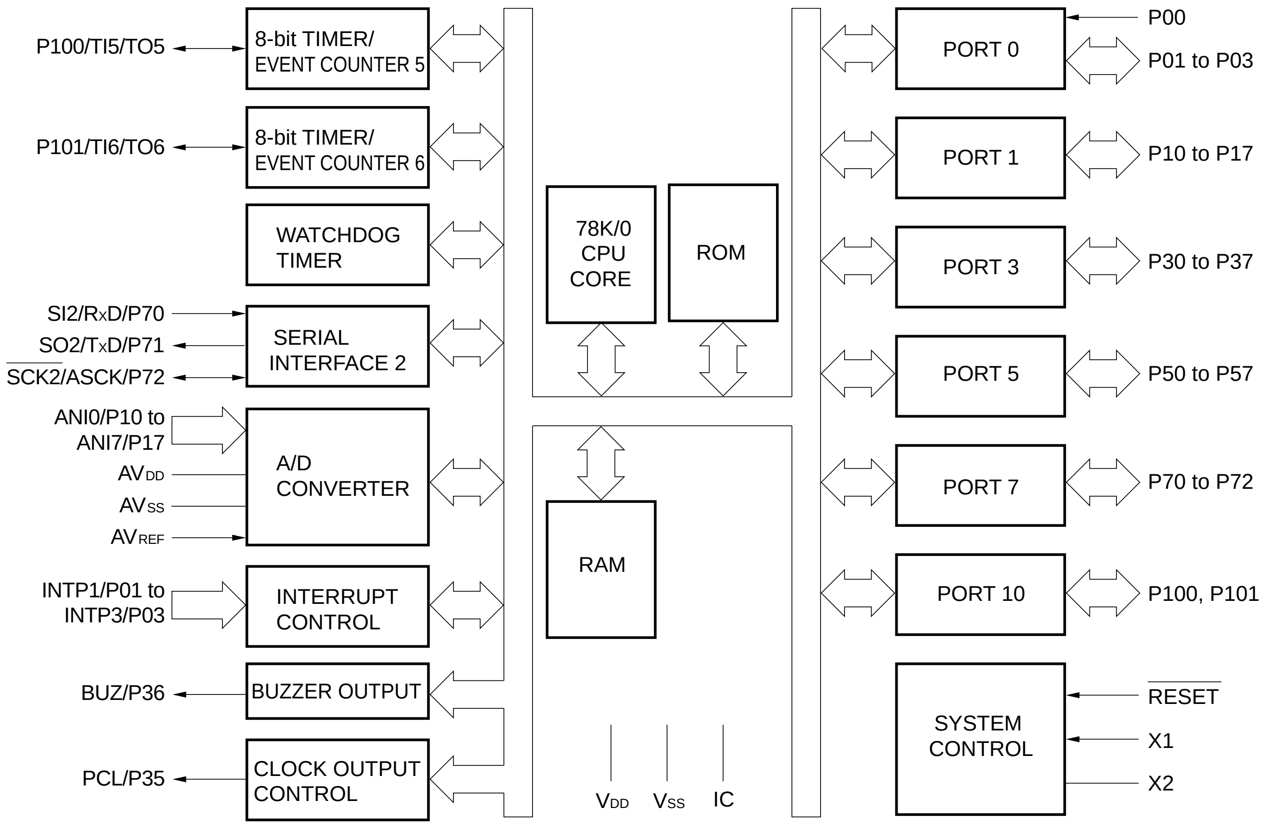
2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

4. Connect NC (Non-connection) pin to V_{SS} for noise protection (It can be left open).

ANI0 to ANI7	:	Analog Input	P100, P101	:	Port10
ASCK	:	Asynchronous Serial Clock	PCL	:	Programmable Clock
AV_{DD}	:	Analog Power Supply	$\overline{RESET}$	:	Reset
AV_{REF}	:	Analog Reference Voltage	RxD	:	Receive Data
AV_{SS}	:	Analog Ground	$\overline{SCK2}$	:	Serial Clock
BUZ	:	Buzzer Clock	SI2	:	Serial Input
IC	:	Internally Connected	SO2	:	Serial Output
INTP1 to INTP3	:	Interrupt from Peripherals	TI5, TI6	:	Timer Input
NC	:	Non-connection	TO5, TO6	:	Timer Output
P00 to P03	:	Port0	TxD	:	Transmit Data
P10 to P17	:	Port1	V_{DD}	:	Power Supply
P30 to P37	:	Port3	V_{SS}	:	Ground
P50 to P57	:	Port5	X1, X2	:	Crystal (Main System Clock)
P70 to P72	:	Port7			

2. BLOCK DIAGRAM



Remark The internal ROM and internal high-speed RAM capacities depend on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	Input/Output	Function		After Reset	Shared by:
P00	Input	Port 0 4-bit input/output port	Input only	Input	—
P01	Input/output		Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	INTP1
P02					INTP2
P03					INTP3
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software. Note		Input	ANI0 to ANI7
P30 to P34	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	—
P35					PCL
P36					BUZ
P37					—
P50 to P57	Input/output	Port 5 8-bit input/output port Can drive up to seven LEDs directly. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	—
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{\text{SCK2}}$/ASCK
P100	Input/output	Port 10 2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	TI5/TO5
P101					TI6/TO6

Note When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for the A/D converter, set the port 1 to the input mode. The on-chip pull-up resistor is automatically disabled.

3.2 Non-port Pins

Pin Name	Input/Output	Function	After Reset	Shared by:
INTP1	Input	External interrupt request input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P01
INTP2				P02
INTP3				P03
SI2	Input	Serial interface serial data input.	Input	P70/RxD
SO2	Output	Serial interface serial data output.	Input	P71/TxD
$\overline{\text{SCK2}}$	Input/Output	Serial interface serial clock input/output.	Input	P72/ASCK
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{\text{SCK2}}$
TI5	Input	External count clock input to 8-bit timer (TM5).	Input	P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO5	Output	8-bit timer (TM5) output.	Input	P100/TI5
TO6		8-bit timer (TM6) output.		P101/TI6
PCL	Output	Clock output. (for main system clock trimming)	Input	P35
BUZ	Output	Buzzer output.	Input	P36
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}.	—	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}.	—	—
$\overline{\text{RESET}}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connect directly to V_{SS}.	—	—
NC	—	Does not internally connected. Connect to V_{SS}. (It can be left open)	—	—

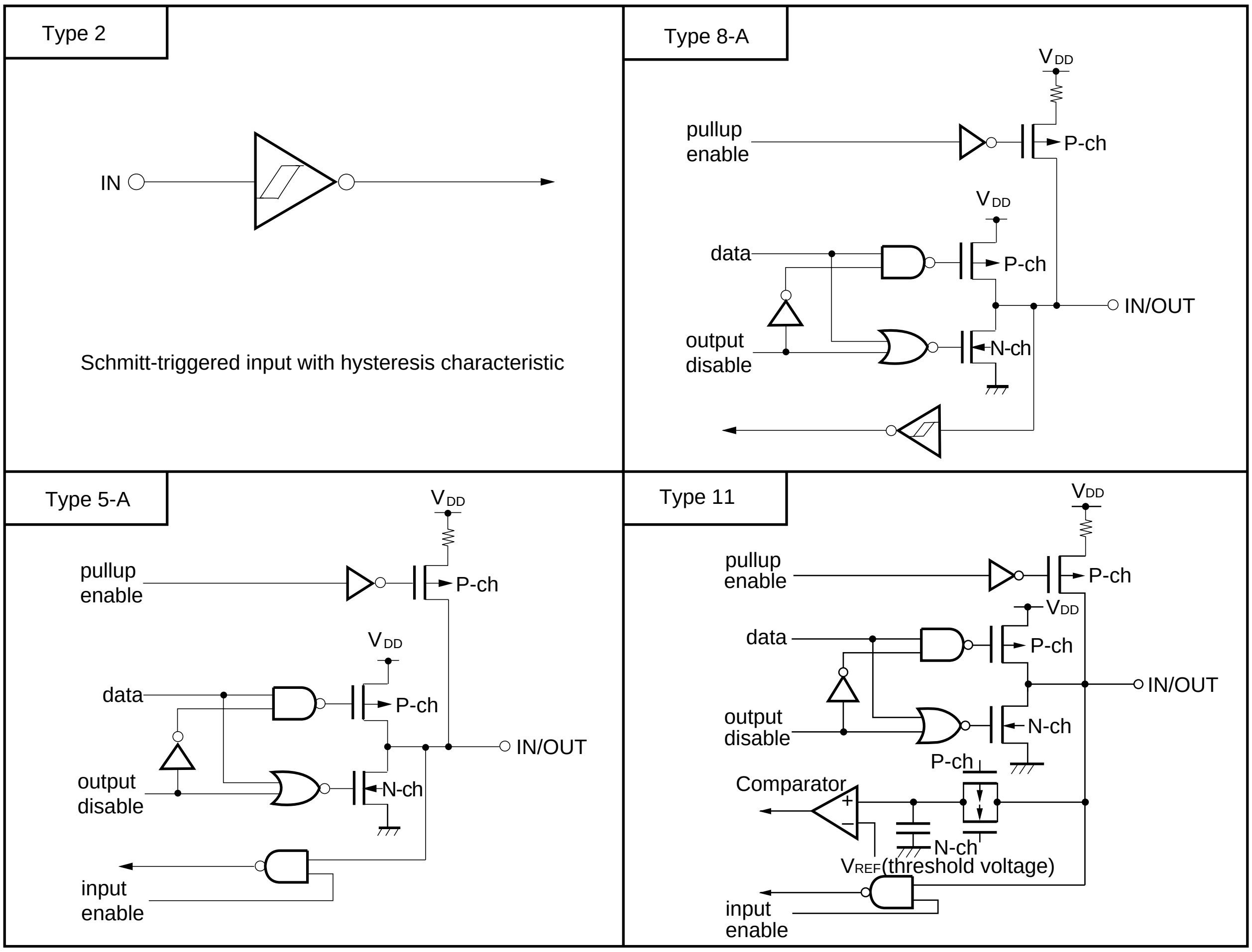
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.
For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P00	2	Input	Connect to V_{SS}.
P01/INTP1	8-A	Input/output	Connect to V_{SS} via a resistor individually.
P02/INTP2			
P03/INTP3			
P10/ANI0 to P17/ANI7	11	Input/output	Connect to V_{DD} or V_{SS} via a resistor individually.
P30 to P32	5-A		
P33, P34	8-A		
P35/PCL	5-A		
P36/BUZ			
P37			
P50 to P57	5-A		
P70/SI2/RxD	8-A		
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P100/TI5/TO5	8-A		
P101/TI6/TO6			
$\overline{RESET}$	2	Input	—
AV_{REF}	—	—	Connect to V_{SS}.
AV_{DD}			Connect to V_{DD}.
AV_{SS}			Connect to V_{SS}.
IC			Connect directly to V_{SS}.
NC			Connect to V_{SS} (It can be left open).

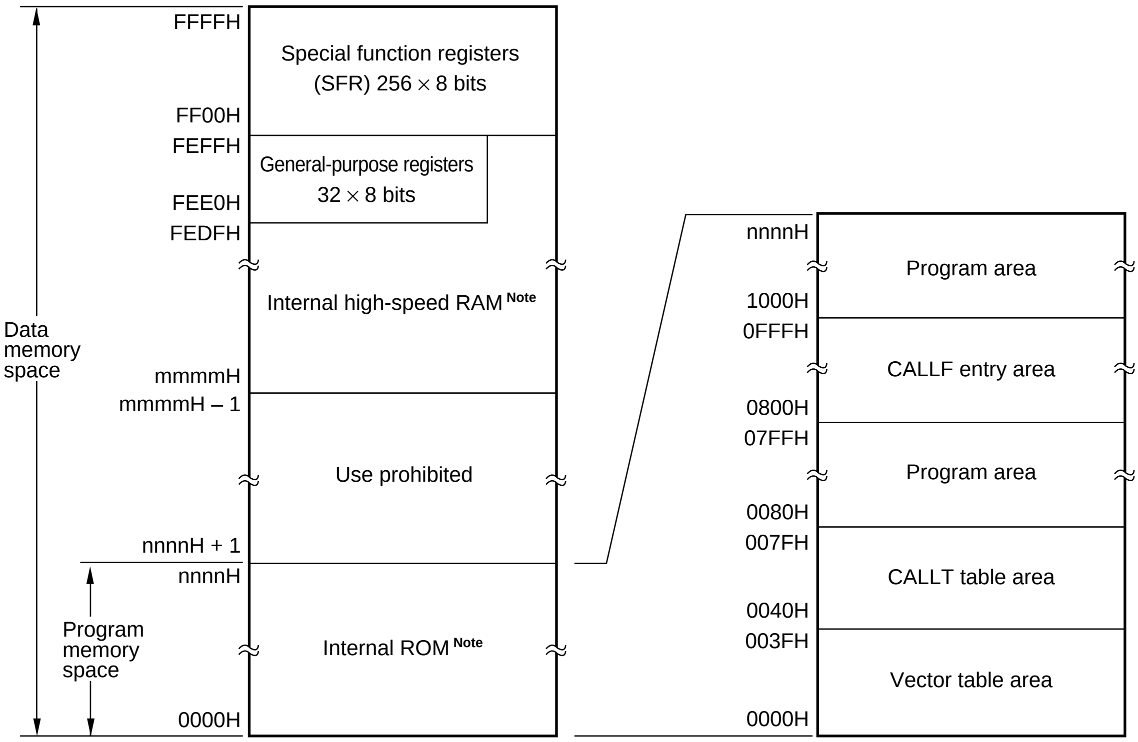
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of the μPD78081(A) and 78082(A) is shown in Figure 4-1.

Figure 4-1. Memory Map



Note The internal ROM and internal high-speed RAM capacities depend on the product (See the following table).

Part Number	Internal ROM Last Address nnnnH	Internal High-speed RAM Start Address mmmmH
μPD78081(A)	1FFFH	FE00H
μPD78082(A)	3FFFH	FD80H

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

Input/output ports are classified into two types.

- CMOS input (P00) : 1
- CMOS input/output (P01 to P03, Port 1, Port 3, Port 5, Port 7, Port 10) : 32

Total : 33

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P00	Input only.
	P01 to P03	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 5	P50 to P57	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. LED can be driven directly up to 7 pins.
Port 7	P70 to P72	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 10	P100, P101	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.

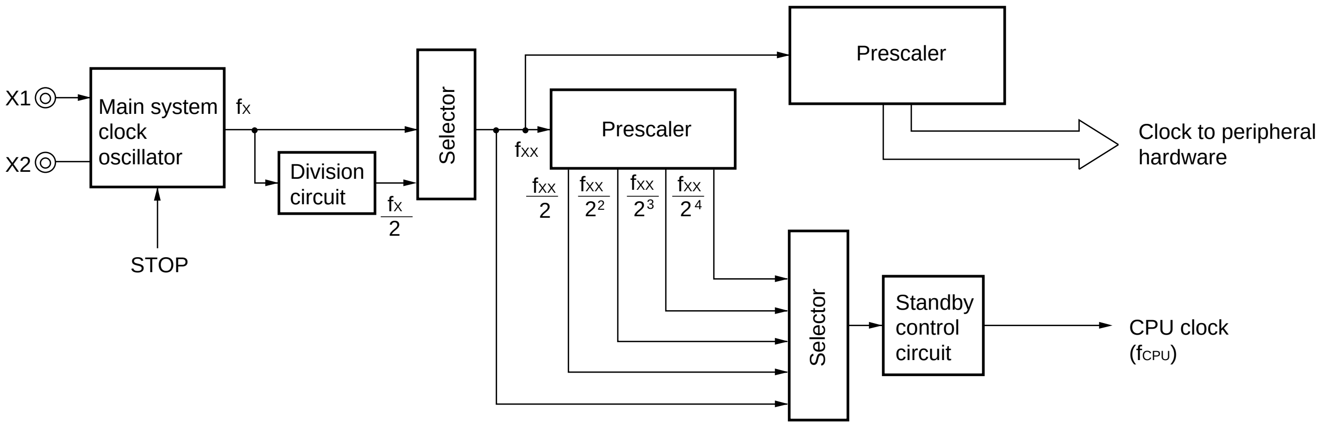
5.2 Clock Generator

Main system clock generator is incorporated.

It is possible to change the minimum instruction execution time.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at main system clock frequency of 5.0 MHz)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

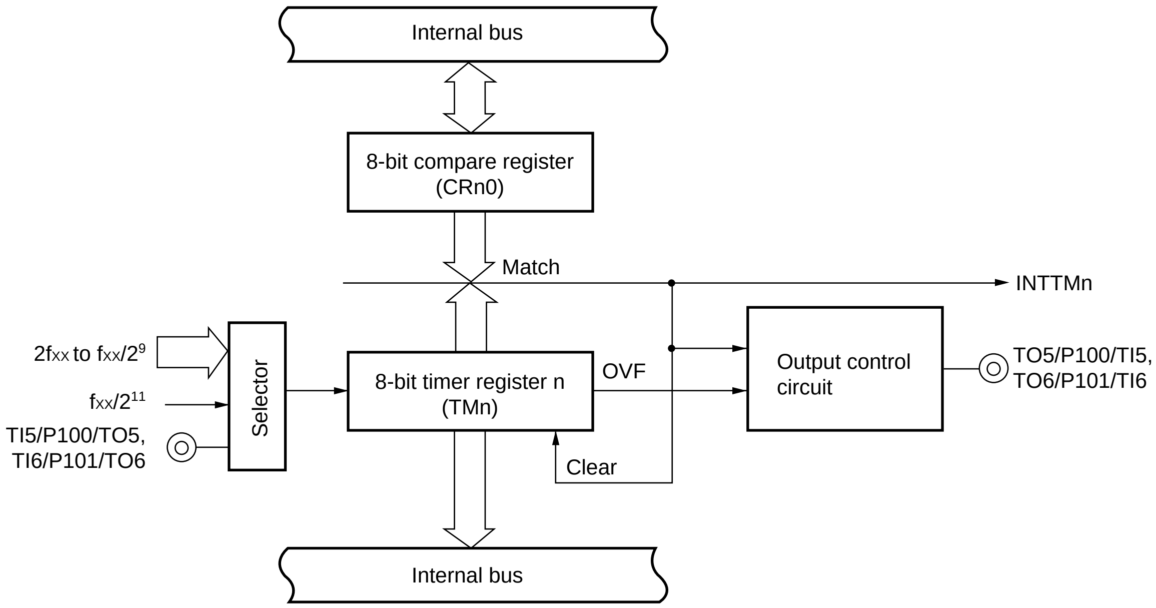
There are the following three timer/event counter channels:

- 8-bit timer/event counter : 2 channels
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

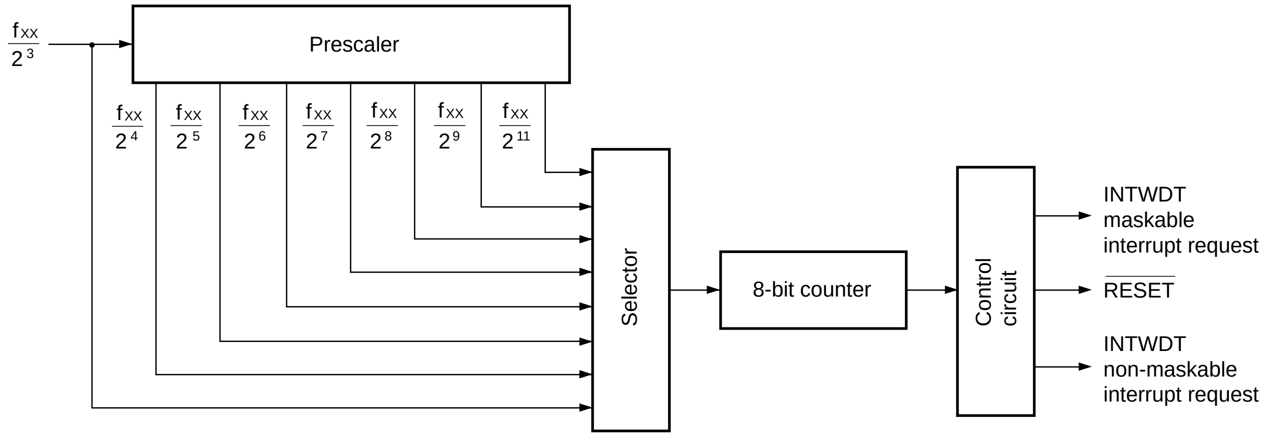
		8-bit Timer/Event Counter 5, 6	Watchdog Timer
Type	Interval timer	2 channels	1 channel
	External event counter	2 channels	—
Function	Timer output	2 outputs	—
	PWM output	2 outputs	—
	Square wave output	2 outputs	—
	Interrupt request	2	1

Figure 5-2. 8-Bit Timer/Event Counter 5, 6 Block Diagram



n = 5, 6

Figure 5-3. Watchdog Timer Block Diagram

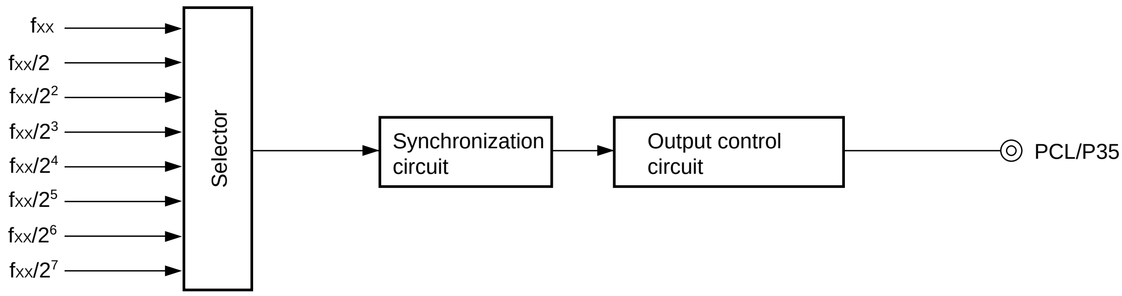


5.4 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (at main system clock frequency of 5.0 MHz)

Figure 5-4. Clock Output Control Circuit Block Diagram

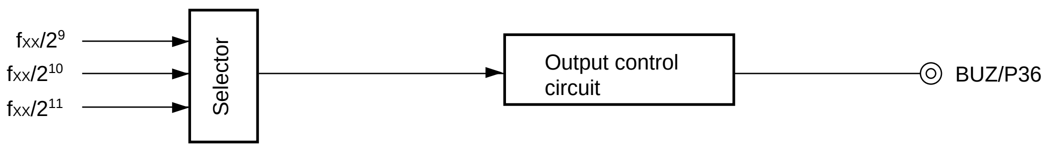


5.5 Buzzer Output Control Circuit

This circuit can output clocks of the following frequencies that can be used for driving buzzers:

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (at main system clock frequency of 5.0 MHz)

Figure 5-5. Buzzer Output Control Circuit Block Diagram



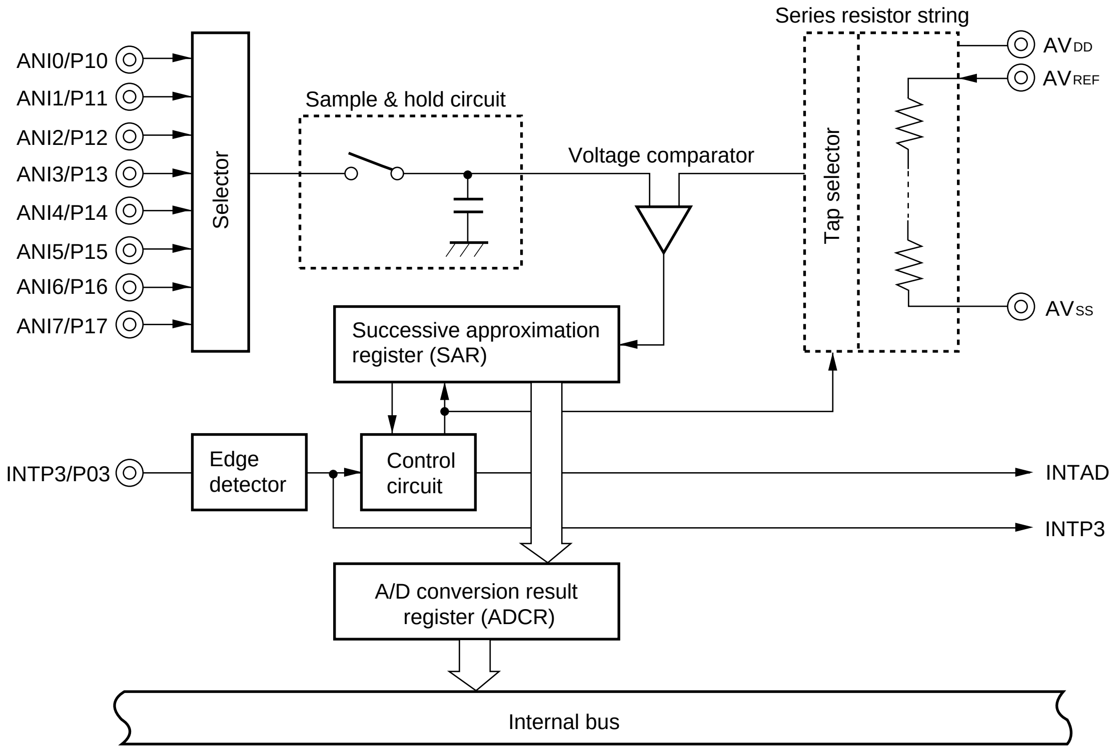
5.6 A/D Converter

The A/D converter consists of eight 8-bit resolution channels.

A/D conversion can be started by the following two methods:

- Hardware starting
- Software starting

Figure 5-6. A/D Converter Block Diagram



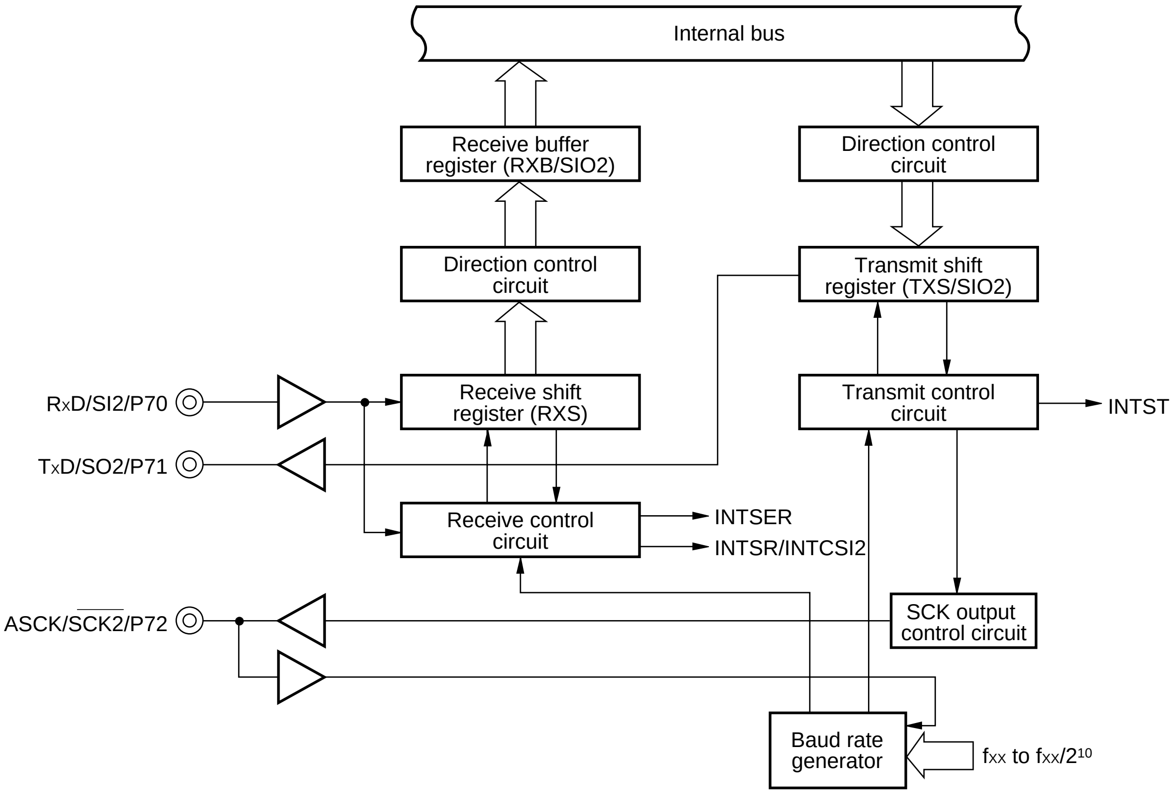
5.7 Serial Interface

There is one on-chip serial interface channel synchronous with the clock.

The serial interface channel 2 operates in the following two modes:

- 3-wire serial I/O mode : Starting bit MSB/LSB switching possible
- Asynchronous serial interface (UART) mode : On-chip dedicated baud rate generator

Figure 5-7. Serial Interface Channel 2 Block Diagram



6. INTERRUPT FUNCTIONS

Interrupt functions include three types and thirteen sources as shown below.

- Non-maskable : 1
- Maskable : 11
- Software : 1

Table 6-1. List of Interrupt Sources

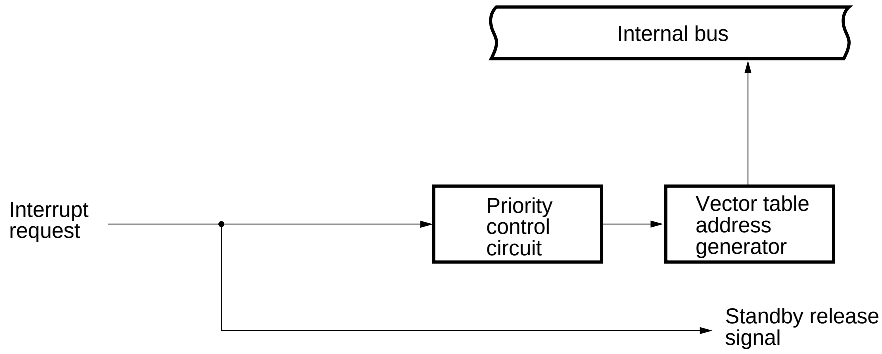
Interrupt Type	Default Priority [Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type [Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (when the watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when the interval timer mode is selected)			(B)
	1	INTP1	Pin input edge detection	External	0008H	(C)
	2	INTP2			000AH	
	3	INTP3			000CH	
	4	INTSER	Occurrence of serial interface channel 2 UART reception error	Internal	0018H	(B)
	5	INTSR	Completion of serial interface channel 2 UART reception		001AH	
		INTCSI2	Completion of serial interface channel 2 3-wire transfer			
	6	INTST	Completion of serial interface channel 2 UART transmission		001CH	
	7	INTAD	Completion of A/D conversion		0028H	
	8	INTTM5	Generation of matching signal of 8-bit timer/event counter 5		002AH	
	9	INTTM6	Generation of matching signal of 8-bit timer/event counter 6		002CH	
Software	—	BRK	Execution of BRK instruction	—	003EH	(D)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 9 is the lowest order.

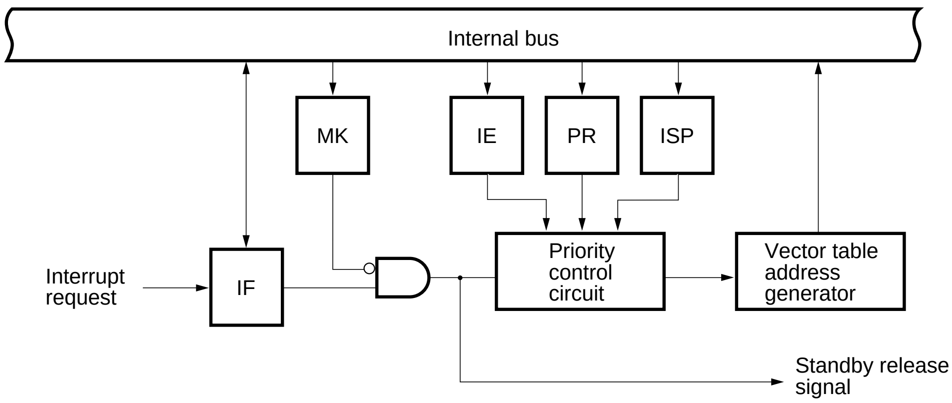
2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt

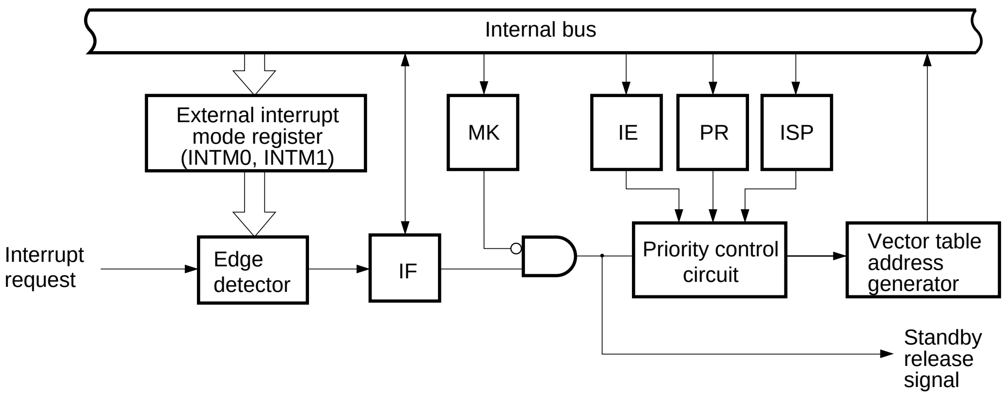
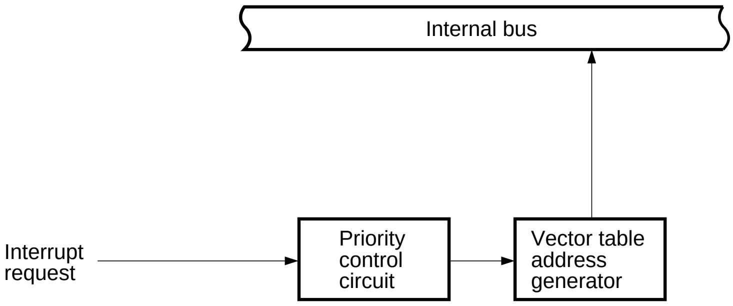


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) Software interrupt



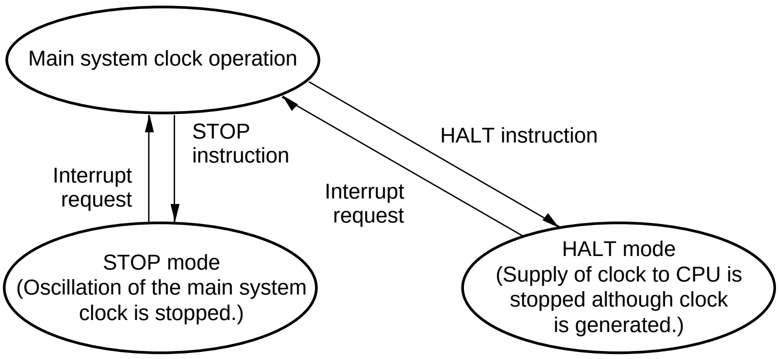
IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

7. STANDBY FUNCTION

The standby function intends to reduce current consumption. It has the following two modes:

- HALT mode : In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode : In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and power consumption becomes extremely small.

Figure 7-1. Standby Function



8. RESET FUNCTION

There are the following two reset methods.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

9. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											

Note Except r = A

2nd Operand / 1st Operand	#byte	A	r	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#word	AX	rp Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

• **Electrical specifications of μPD78081(A) and 78082(A) (1/11)**

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pins	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total of P10 to P17, P50 to P54, P70 to P72, P100, P101		–15	mA
		Total of P01 to P03, P30 to P37, P55 to P57		–15	mA
Output current, low	I_{OL} Note	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total of P50 to P54	Peak value	100	mA
			r.m.s. value	70	mA
		Total of P55 to P57	Peak value	100	mA
			r.m.s. value	70	mA
		Total of P10 to P17, P70 to P72, P100, P101	Peak value	50	mA
			r.m.s. value	20	mA
		Total of P01 to P03, P30 to P37	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] $\times \sqrt{\text{Duty}}$

Caution If the absolute maximum rating of even one of the above parameters is exceeded, the quality of the product may be degraded. The absolute maximum ratings are therefore the rated values that may, if exceeded, physically damage the product. Be sure to use the product with all the absolute maximum ratings observed.

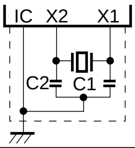
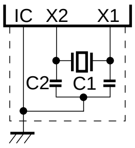
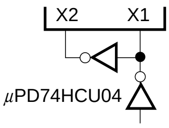
Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz, Unmeasured pins returned to 0 V.	P01 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101			15	pF

Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

- **Electrical specifications of μPD78081(A) and 78082(A) (2/11)**

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		5.0	MHz
		X1 input high-/low-level widths (t_{XH}, t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to AC Characteristics.

2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Caution When using the oscillation circuit of the main system clock, wire the portion enclosed in broken lines in the figures as follows to avoid adverse influence on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

- **Electrical specifications of μPD78081(A) and 78082(A) (3/11)**

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P30 to P32, P35 to P37, P50 to P57, P71	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P30 to P32, P35 to P37, P50 to P57, P71	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00 to P03, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL}	P50 to P57	V_{DD} = 2.0 to 4.5 V, I_{OL} = 10 mA			0.8	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P30 to P37, P70 to P72, P100, P101	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
Input leak current, high	I_{LIH1}	V_{IN} = V_{DD}	P00 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2			20	μA
Input leak current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leak current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leak current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistance	R	V_{IN} = 0 V	P01 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101	15	40	90	kΩ

Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

- **Electrical specifications of μPD78081(A) and 78082(A) (4/11)**

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ±10% Note 4		4.5	13.5	mA
			V_{DD} = 3.0 V ±10% Note 5		0.7	2.1	mA
			V_{DD} = 2.0 V ±10% Note 5		0.4	1.2	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ±10% Note 4		8.0	24.0	mA
			V_{DD} = 3.0 V ±10% Note 5		0.9	2.7	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ±10%		1.4	4.2	mA
			V_{DD} = 3.0 V ±10%		0.5	1.5	mA
			V_{DD} = 2.0 V ±10%		280	840	μA
		5.0-MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ±10%		1.6	4.8	mA
			V_{DD} = 3.0 V ±10%		0.65	1.95	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. Not including AV_{REF} and AV_{DD} currents or port currents (including current flowing into on-chip pull-up resistors).

2. f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H).

3. f_{XX} = f_X operation (when oscillation mode selection register (OSMS) is set to 01H).

4. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when processor clock control register (PCC) is set to 04H).

Remark f_{XX} : Main system clock frequency (f_X or f_X/2)

f_X : Main system clock oscillation frequency

- **Electrical specifications of μPD78081(A) and 78082(A) (5/11)**

AC Characteristics

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	$f_{XX} = f_X/2$ Note 1	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
				2.0		64	μs
		$f_{XX} = f_X$ Note 2	3.5 V ≤ V_{DD} ≤ 5.5 V	0.4		32	μs
			2.7 V ≤ V_{DD} < 3.5 V	0.8		32	μs
TI5, TI6 input frequency	f_{TI}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI5, TI6 input high-/ low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high-/ low-level widths	t_{INTH}, t_{INTL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

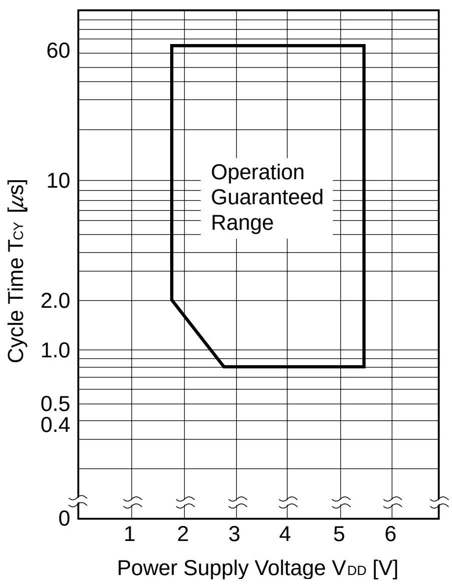
Notes 1. When oscillation mode selection register (OSMS) is set to 00H.

2. When OSMS is set to 01H.

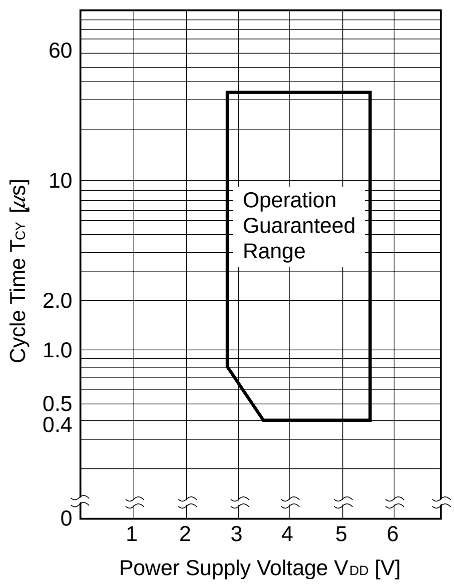
Remark f_{XX} : Main system clock frequency (f_X or $f_X/2$)

f_X : Main system clock oscillation frequency

T_{CY} vs V_{DD} (Main System Clock $f_{XX} = f_X/2$ Operation)



T_{CY} vs V_{DD} (Main System Clock $f_{XX} = f_X$ Operation)



- **Electrical specifications of μPD78081(A) and 78082(A) (6/11)**

(2) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3,200			ns
			4,800			ns
$\overline{SCK2}$ high-/low-level widths	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI1}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO1}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of $\overline{SCK2}$ and SO2 output lines.

(b) 3-wire serial I/O mode ($\overline{SCK2}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3,200			ns
				4,800			ns
$\overline{SCK2}$ high-/low-level widths	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1,600			ns
				2,400			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI2}			400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO2}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK2}$ rise/fall time	t_{R2}, t_{F2}					1,000	ns

Note C is the load capacitance of SO2 output line.

- **Electrical specifications of μPD78081(A) and 78082(A) (7/11)**

(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.5\ V \leq V_{DD} \leq 5.5\ V$			78,125	bps
		$2.7\ V \leq V_{DD} < 4.5\ V$			39,063	bps
		$2.0\ V \leq V_{DD} < 2.7\ V$			19,531	bps
					9,766	bps

(d) UART mode (External clock input)

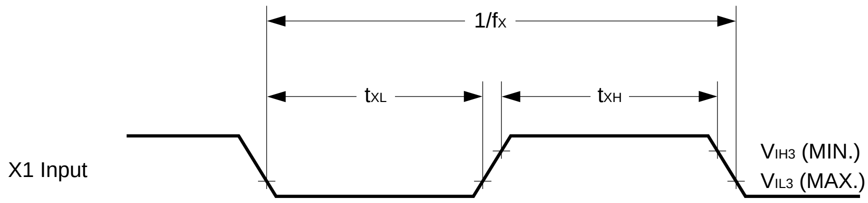
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	$4.5\ V \leq V_{DD} \leq 5.5\ V$	800			ns
		$2.7\ V \leq V_{DD} < 4.5\ V$	1,600			ns
		$2.0\ V \leq V_{DD} < 2.7\ V$	3,200			ns
			4,800			ns
ASCK high-/low-level widths	t_{KH3}, t_{KL3}	$4.5\ V \leq V_{DD} \leq 5.5\ V$	400			ns
		$2.7\ V \leq V_{DD} < 4.5\ V$	800			ns
		$2.0\ V \leq V_{DD} < 2.7\ V$	1,600			ns
			2,400			ns
Transfer rate		$4.5\ V \leq V_{DD} \leq 5.5\ V$			39,063	bps
		$2.7\ V \leq V_{DD} < 4.5\ V$			19,531	bps
		$2.0\ V \leq V_{DD} < 2.7\ V$			9,766	bps
					6,510	bps
ASCK rise/fall time	t_{R3}, t_{F3}				1,000	ns

• **Electrical specifications of μPD78081(A) and 78082(A) (8/11)**

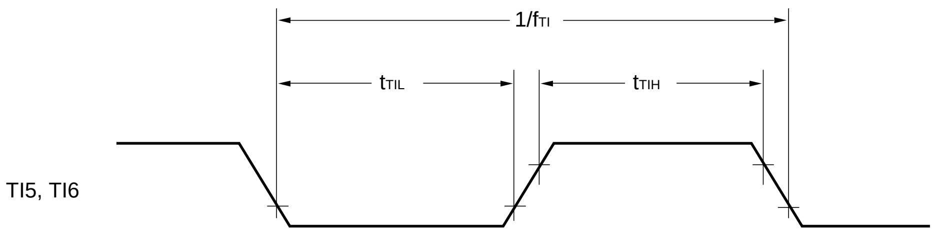
AC Timing Test Points (excluding X1 Input)



Clock Timing



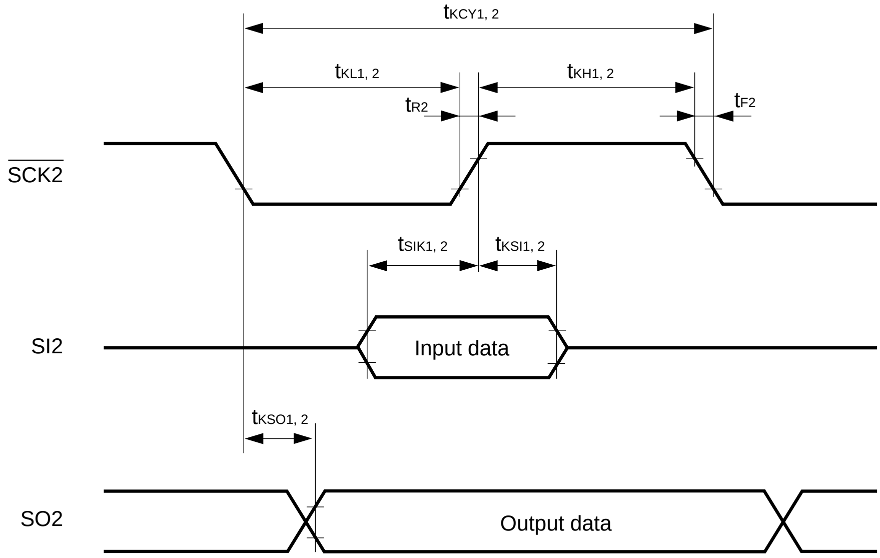
TI Timing



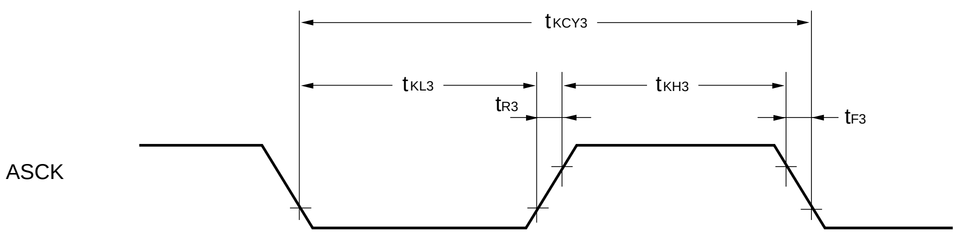
- **Electrical specifications of μPD78081(A) and 78082(A) (9/11)**

Serial Transfer Timing

3-wire serial I/O mode :



UART mode (external clock input) :



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		2.7 V ≤ AV_{REF} ≤ AV_{DD}			0.6	%
		1.8 V ≤ AV_{REF} < 2.7 V			1.4	%
Conversion time	t_{CONV}	2.0 V ≤ AV_{DD} ≤ 5.5 V	19.1		200	μs
		1.8 V ≤ AV_{DD} < 2.0 V	38.2		200	μs
Sampling time	t_{SAMP}		12/fxx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{AIREF}		4	14		kΩ

Note Overall error excluding quantization error (±1/2LSB). It is indicated as a ratio to the full-scale value.

Remark f_{XX} : Main system clock frequency (f_X or f_X/2)
f_X : Main system clock oscillation frequency

- **Electrical specifications of μPD78081(A) and 78082(A) (10/11)**

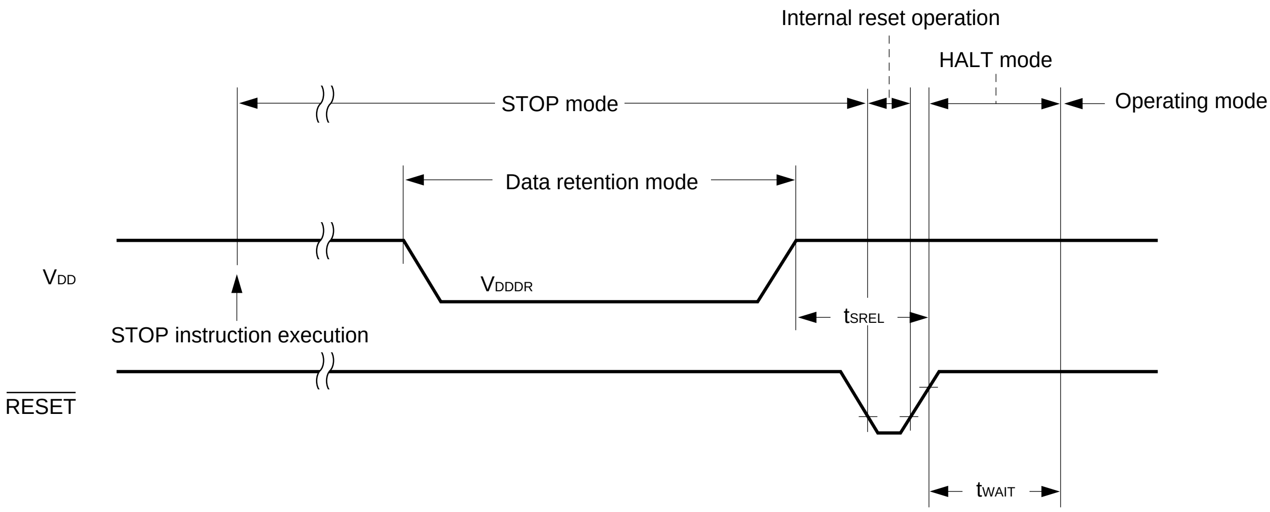
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/fx$		ms
		Release by interrupt request		**Note**		ms

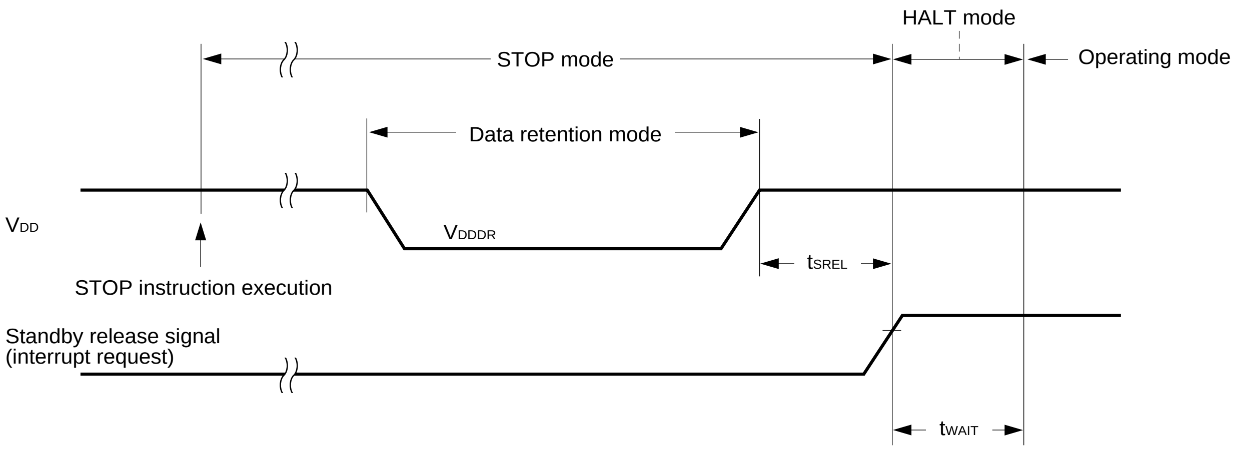
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{12}/f_{XX}$ and $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ is possible.

Remark f_{XX} : Main system clock frequency (f_X or $f_X/2$)
f_X : Main system clock oscillation frequency

Data Retention Timing (STOP mode release by $\overline{RESET}$)

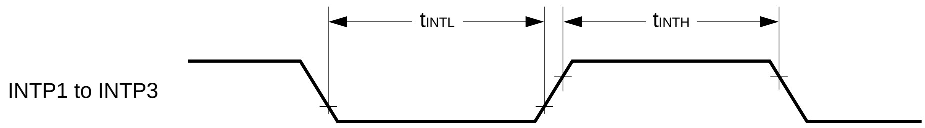


Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)

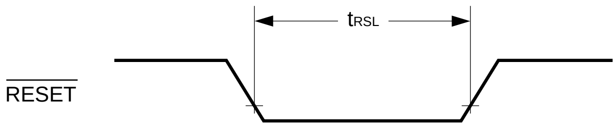


- **Electrical specifications of μPD78081(A) and 78082(A) (11/11)**

Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



- **Electrical specifications of μPD78081(A2) (1/10)**

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pins	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total of P10 to P17, P50 to P54, P70 to P72, P100, P101		–15	mA
		Total of P01 to P03, P30 to P37, P55 to P57		–15	mA
Output current, low	I_{OL} Note	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total of P50 to P54	Peak value	100	mA
			r.m.s. value	70	mA
		Total of P55 to P57	Peak value	100	mA
			r.m.s. value	70	mA
		Total of P10 to P17, P70 to P72, P100, P101	Peak value	50	mA
			r.m.s. value	20	mA
		Total of P01 to P03, P30 to P37	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T_A			–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] $\times\sqrt{\text{Duty}}$

Caution If the absolute maximum rating of even one of the above parameters is exceeded, the quality of the product may be degraded. The absolute maximum ratings are therefore the rated values that may, if exceeded, physically damage the product. Be sure to use the product with all the absolute maximum ratings observed.

Permissible Pin Sink Current Characteristics with Overvoltage Applied

Pending

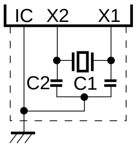
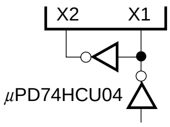
Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz, Unmeasured pins returned to 0 V.	P01 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101			15	pF

Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

- **Electrical specifications of μPD78081(A2) (2/10)**

Main System Clock Oscillator Characteristics (T_A = –40 to +125°C, V_{DD} = 5 V ±10%)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0		7.0	MHz
		Oscillation stabilization time Note 2				10	ms
External clock		X1 input frequency (f_X) Note 1		1.0		7.0	MHz
		X1 input high-/low-level widths (t_{XH}, t_{XL})		64		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to AC Characteristics.

2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Caution When using the oscillation circuit of the main system clock, wire the portion enclosed in broken lines in the figure as follows to avoid adverse influence on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

- **Electrical specifications of μPD78081(A2) (3/10)**

DC Characteristics (T_A = –40 to +125°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P30 to P32, P35 to P37, P50 to P57	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P33, P34, P70 to P72, P100, P101, $\overline{RESET}$	0.9 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2	V_{DD} – 0.2		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P30 to P32, P35 to P37, P50 to P57	0		0.3 V_{DD}	V
	V_{IL2}	P00 to P03, P33, P34, P70 to P72, P100, P101, $\overline{RESET}$	0		0.16 V_{DD}	V
	V_{IL3}	X1, X2	0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
		I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	P50 to P57; I_{OL} = 15 mA		0.4	2.2	V
		P01 to P03, P10 to P17, P30 to P37, P70 to P72, P100, P101; I_{OL} = 1.6 mA			0.45	V
		P01 to P03, P10 to P17, P30 to P37, P70 to P72, P100, P101; I_{OL} = 400 μA			0.5	V
Input leak current, high	I_{LIH1}	V_{IN} = V_{DD}; P00 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101, $\overline{RESET}$			10	V
	I_{LIH2}	V_{IN} = V_{DD}; X1, X2			20	μA
Input leak current, low	I_{LIL1}	V_{IN} = 0 V; P00 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101, $\overline{RESET}$			–10	μA
	I_{LIL2}	V_{IN} = 0 V; X1, X2			–20	μA
Output leak current, high	I_{LOH}	V_{OUT} = V_{DD}			10	μA
Output leak current, low	I_{LOL}	V_{OUT} = 0 V			–10	μA
Software pull-up resistance	R	V_{IN} = 0 V; P01 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101	15	40	120	kΩ
Supply current Note 1	I_{DD1}	7.0-MHz crystal oscillation operating mode (f_{XX} = 3.5 MHz) Notes 2, 3		9.0	29.0	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz) Notes 2, 3		5.5	16.5	mA
	I_{DD2}	7.0-MHz crystal oscillation HALT mode (f_{XX} = 3.5 MHz) Note 2		1.5	7.2	mA
		5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2		1.2	6.5	mA
	I_{DD3}	STOP mode		0.1	1,000	μA

Notes 1. Not including AV_{REF} and AV_{DD} currents or port currents (including current flowing into on-chip pull-up resistors).

2. f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H).

3. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

Remarks 1. f_{XX} : Main system clock frequency (f_X or f_X/2)

2. f_X : Main system clock oscillation frequency

3. Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

- **Electrical specifications of μPD78081(A2) (4/10)**

AC Characteristics

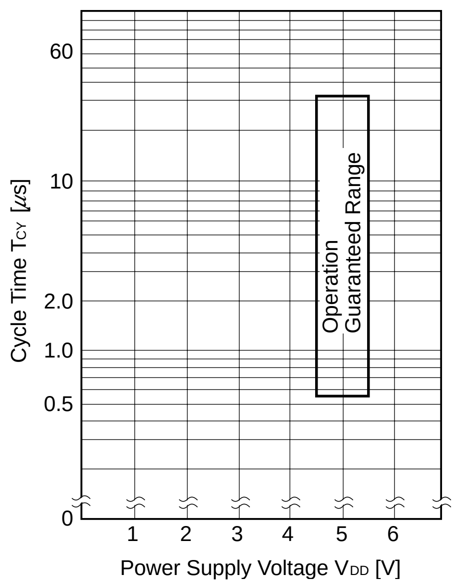
(1) Basic Operation (T_A = –40 to +125°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	$f_{XX} = f_X/2$ Note	0.57		32	μs
TI5, TI6 input frequency	f_{TI}		0		2	kHz
TI5, TI6 input high-/low-level widths	t_{TIH}, t_{TIL}		200			ns
Interrupt request input high-/low-level widths	t_{INTH}, t_{INTL}		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

Note When oscillation mode selection register (OSMS) is set to 00H.

Remark f_{XX} : Main system clock frequency (f_X or $f_X/2$)
f_X : Main system clock oscillation frequency

T_{CY} vs V_{DD}
(Main System Clock $f_{XX} = f_X/2$ Operation)



- **Electrical specifications of μPD78081(A2) (5/10)**

(2) Serial Interface (T_A = –40 to +125°C, V_{DD} = 5 V ±10%)

(a) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY1}		1,000			ns
$\overline{SCK2}$ high-/low-level widths	t_{KH1}, t_{KL1}		t_{KCY1}/2 – 100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK1}		150			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI1}		500			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO1}	C = 100 pF **Note**			400	ns

Note C is the load capacitance of $\overline{SCK2}$ and SO2 output lines.

(b) 3-wire serial I/O mode ($\overline{SCK2}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY2}		1,000			ns
$\overline{SCK2}$ high-/low-level widths	t_{KH2}, t_{KL2}		500			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK2}		150			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI2}		500			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO2}	C = 100 pF **Note**			400	ns
$\overline{SCK2}$ rise/fall time	t_{R2}, t_{F2}				1,000	ns

Note C is the load capacitance of SO2 output line.

- **Electrical specifications of μPD78081(A2) (6/10)**

(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					76,923	bps

(d) UART mode (External clock input)

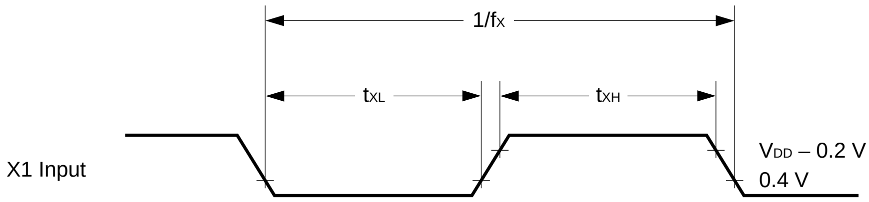
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}		1,000			ns
ASCK high-/low-level widths	t_{KH3}, t_{KL3}		500			ns
Transfer rate					38,462	bps
ASCK rise/fall time	t_{R3}, t_{F3}				1,000	ns

• **Electrical specifications of μPD78081(A2) (7/10)**

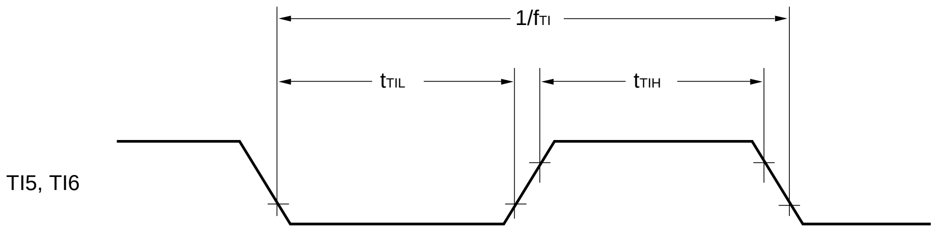
AC Timing Test Points (excluding X1 Input)



Clock Timing



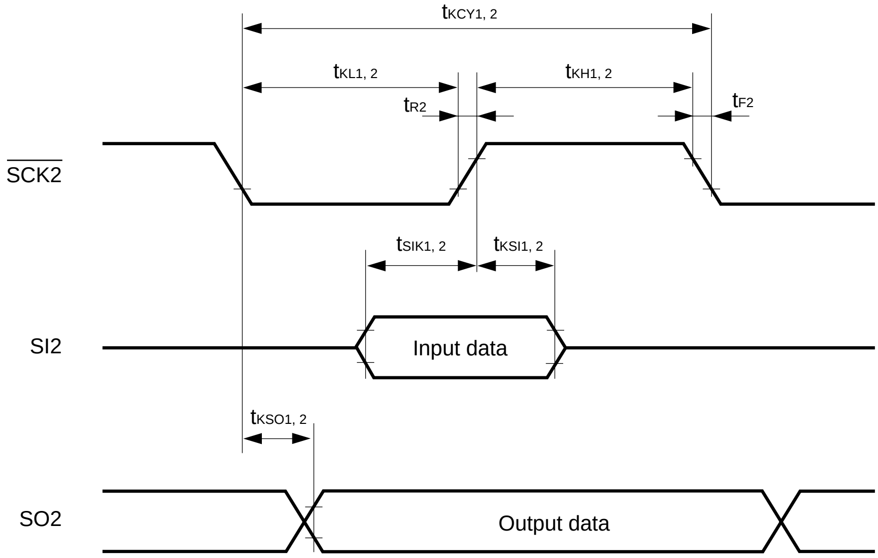
TI Timing



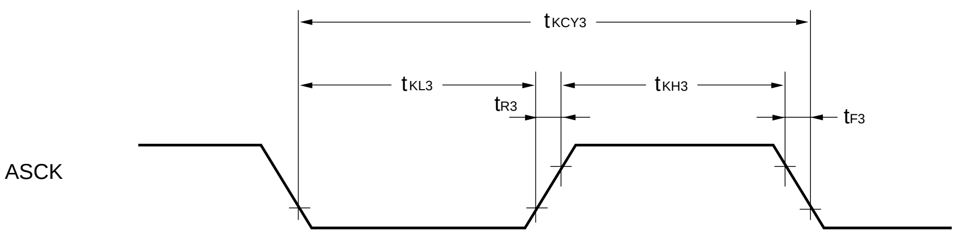
- **Electrical specifications of μPD78081(A2) (8/10)**

Serial Transfer Timing

3-wire serial I/O mode :



UART mode (external clock input) :



A/D Converter Characteristics (T_A = –40 to +125°C, AV_{DD} = V_{DD} = 5 V ±10%, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		4.5 V ≤ AV_{REF} ≤ AV_{DD}			1.0	%
Conversion time	t_{CONV}		23.8		100	μs
Sampling time	t_{SAMP}		12/fxx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{AIREF}		4	14		kΩ

Note Overall error excluding quantization error (±1/2LSB). It is indicated as a ratio to the full-scale value.

Remark f_{XX} : Main system clock frequency (f_X or f_X/2)
f_X : Main system clock oscillation frequency

- **Electrical specifications of μPD78081(A2) (9/10)**

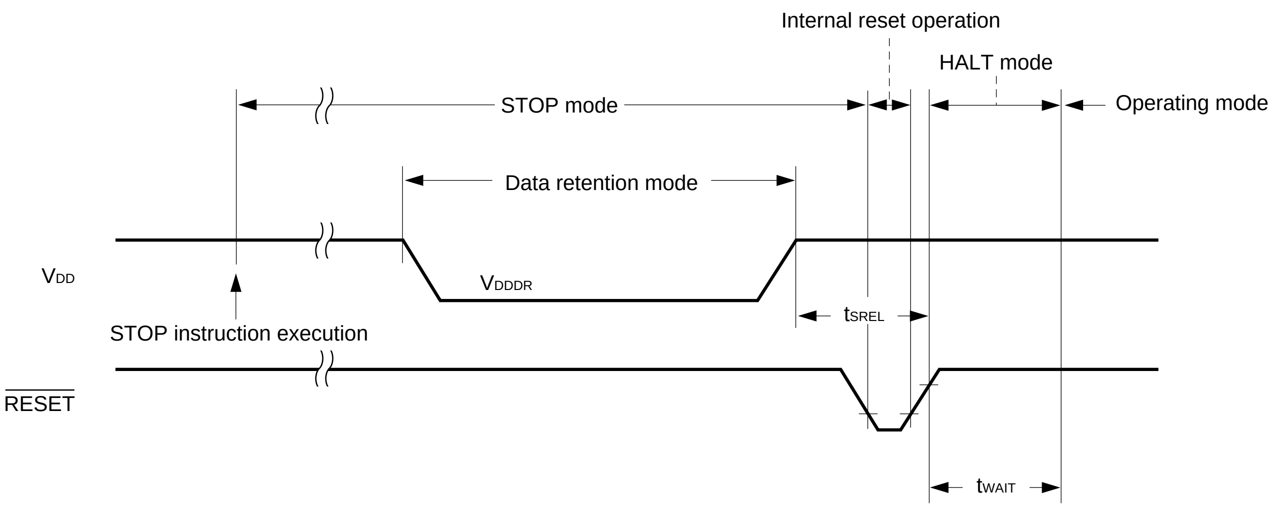
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +125°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		4.5		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 4.5 V		0.1	1,000	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

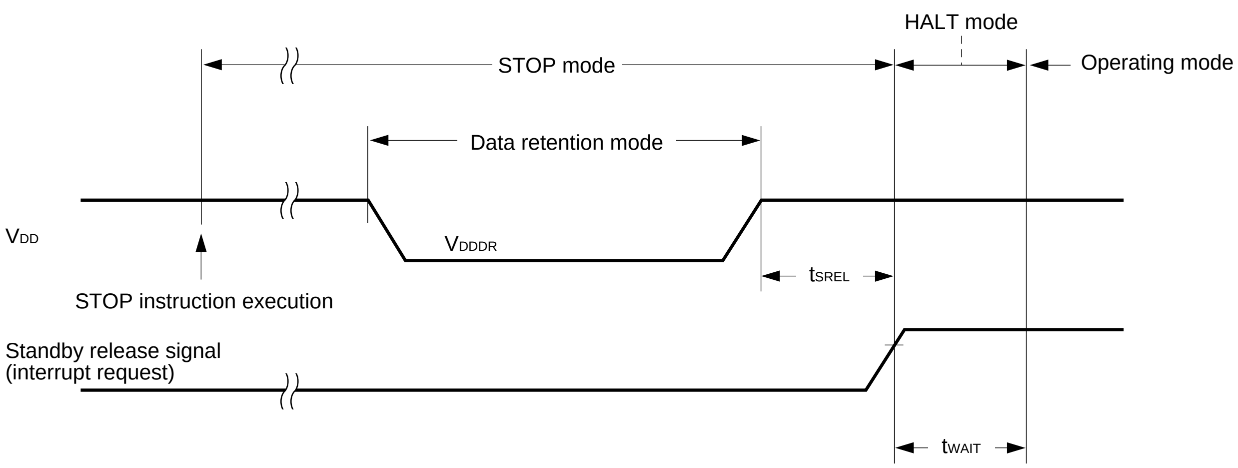
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{12}/f_{XX}$ and $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ is possible.

Remark f_{XX} : Main system clock frequency (f_X or $f_X/2$)
f_X : Main system clock oscillation frequency

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)

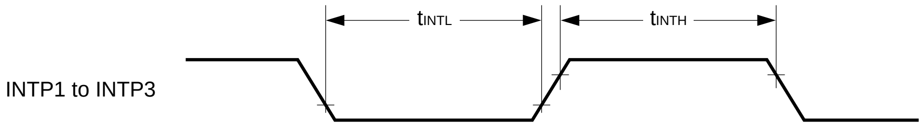


Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)

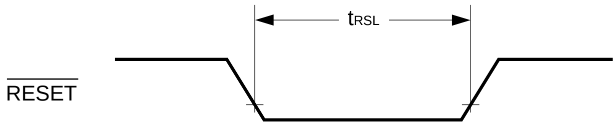


- **Electrical specifications of μPD78081(A2) (10/10)**

Interrupt Request Input Timing



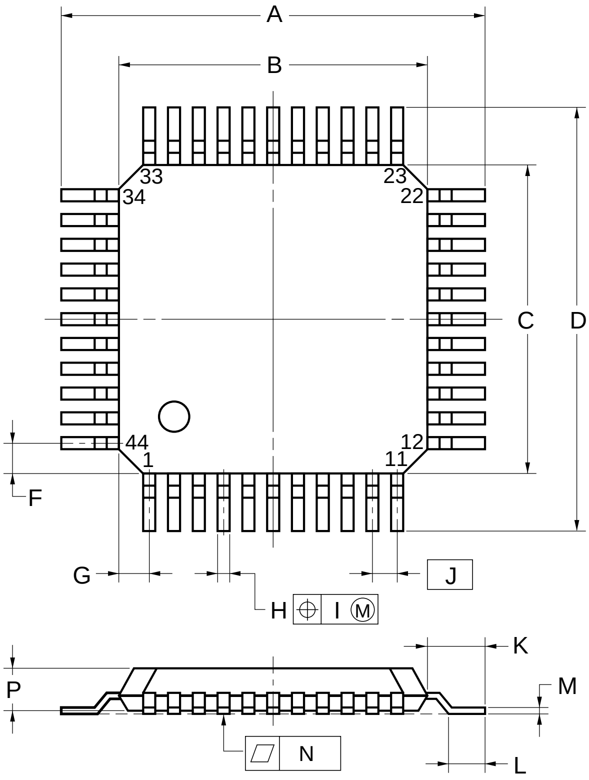
$\overline{\text{RESET}}$ Input Timing



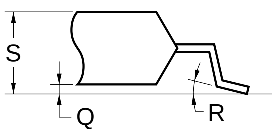
11. PACKAGE DRAWINGS

μPD78081GB(A)-×××-3B4, 78082GB(A)-×××-3B4, 78081GB(A2)-×××-3B4

44 PIN PLASTIC QFP (□10)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

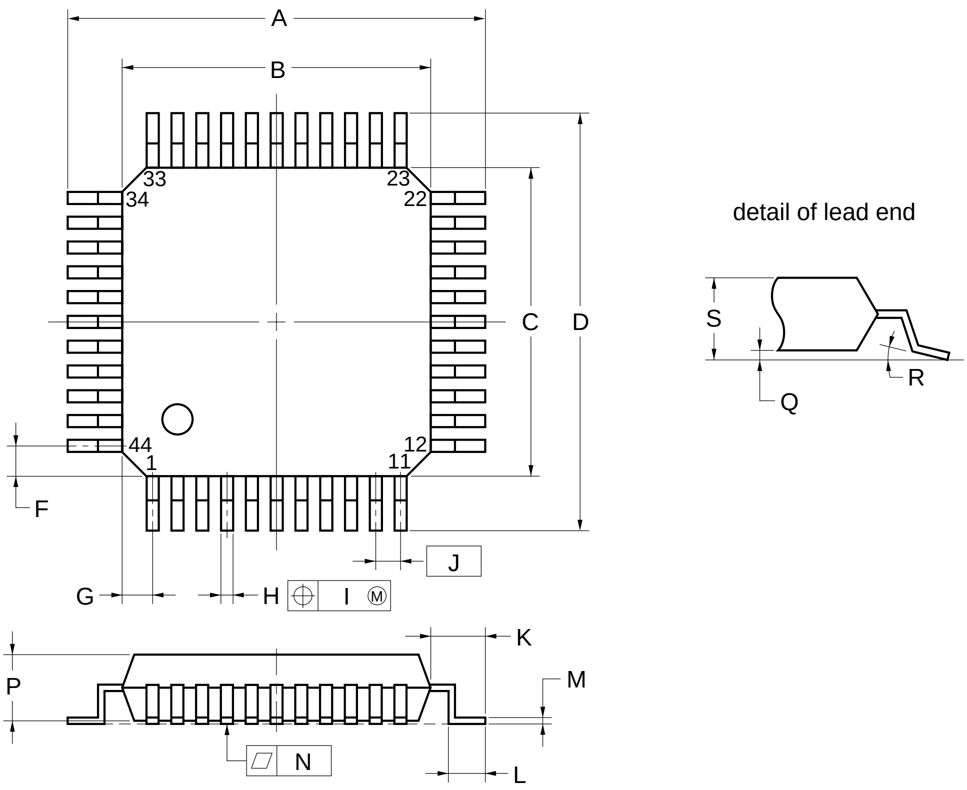
Remark The shape and material of ES versions are the same as those of mass-produced versions.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P44GB-80-3B4-3

μPD78081GB(A)-××× -3BS-MTX, 78082GB(A)-××× -3BS-MTX

44 PIN PLASTIC QFP (□10)



NOTE

Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	$0.520^{+0.008}_{-0.009}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.2	$0.520^{+0.008}_{-0.009}$
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.06}_{-0.05}$	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS

12. RECOMMENDED SOLDERING CONDITIONS

μPD78081(A) and 78082(A) should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, consult our sales representative.

Table 12-1. Surface Mounting Type Soldering Conditions

μPD78081GB(A)-×××-3B4 : 44-pin plastic QFP (10 × 10 mm)
μPD78082GB(A)-×××-3B4 : 44-pin plastic QFP (10 × 10 mm)
μPD78081GB(A2)-×××-3B4 : 44-pin plastic QFP (10 × 10 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (at 210°C or higher), Number of reflow processes: 3 max.	IR35-00-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (at 200°C or higher), Number of reflow processes: 3 max.	VP15-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or below, Number of flow processes: once, Preheating temperature: 120°C or below (package surface temperature)	WS60-00-1
Pin partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per device side)	—

Cautions 1. Use of more than one soldering method should be avoided (except for the pin partial heating method).

2. Because production of the μPD78081GB(A)-×××-3BS-MTX and 78082GB(A)-×××-3BS-MTX is still in a planning stage, their soldering conditions are pending.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available to support development of systems using the μPD78081(A) and 78082(A).

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	Assembler package common to the 78K/0 Series
CC78K/0 Notes 1, 2, 3, 4	C compiler package common to the 78K/0 Series
DF78083 Notes 1, 2, 3, 4	Device file used for the μPD78083 Subseries
CC78K/0-L Notes 1, 2, 3, 4	C compiler library source file common to the 78K/0 Series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P083GB	Programmer adapter connected to the PG-1500
PG-1500 Controller Notes 1, 2	Control program for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator common to the 78K/0 Series
IE-78000-R-A	In-circuit emulator common to the 78K/0 Series (for integrated debugger)
IE-78000-R-BK	Break board common to the 78K/0 Series
IE-78078-R-EM	Emulation board common to the μPD78078 Subseries
EP-78083GB-R	Emulation probe for the μPD78083 Subseries
EV-9200G-44	Socket mounted on the target system board prepared for 44-pin plastic QFP
SM78K0 Notes 5, 6, 7	System simulator common to the 78K/0 Series
ID78K0 Notes 4, 5, 6, 7	Integrated debugger for the IE-78000-R-A
SD78K/0 Notes 1, 2	Screen debugger for the IE-78000-R
DF78083 Notes 1, 2, 5, 6, 7	Device file used for the μPD78083 Subseries

Notes 1. Based on PC-9800 Series (MS-DOS™)
2. Based on IBM PC/AT™ and its compatibles (PC DOS™/IBM DOS™/MS-DOS)
3. Based on HP9000 Series 300™ (HP-UX™)
4. Based on HP9000 Series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS4800 Series (EWS-UX/V)
5. Based on PC-9800 Series (MS-DOS + Windows™)
6. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows)
7. Based on NEWS™ (NEWS-OS™)

Remarks 1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.
2. Use the RA78K/0, CC78K/0, SM78K0, ID78K0, and SD78K/0 in combination with the DF78083.

Real-Time OS

MX78K0 **Notes 1, 2, 3, 4**	OS used for the 78K/0 Series

Fuzzy Inference Development Support System

FE9000 **Note 1**/FE9200 **Note 5**	Fuzzy knowledge data input tool
FT9080 **Note 1**/FT9085 **Note 2**	Translator
FI78K0 **Notes 1, 2**	Fuzzy inference module
FD78K0 **Notes 1, 2**	Fuzzy inference debugger

Notes 1. Based on PC-9800 Series (MS-DOS)
2. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS)
3. Based on HP9000 Series 300 (HP-UX)
4. Based on HP9000 Series 700 (HP-UX), SPARCstation (SunOS), and EWS4800 Series (EWS-UX/V)
5. Based on IBM PC/AT (PC DOS/IBM DOS/MS-DOS + Windows)

Remark Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD78083 Subseries User's Manual	U12176J	IEU-1407
μPD78081(A), 78082(A) Data Sheet	U12436J	This document
μPD78P083(A) Data Sheet	U12175J	U12175E
78K/0 Series User's Manual Instructions	U12326J	IEU-1372
78K/0 Series Instruction Table	U10903J	—
78K/0 Series Instruction Set	U10904J	—
μPD78083 Subseries Special Function Register Table	IEM-5599	—
78K/0 Series Application Note Fundamental (III)	IEA-767	U10182E

Documents Related to Development Tools (User's Manual) (1/2)

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	—
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		U11376J	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78078-R-EM		U10775J	U10775E
EP-78083		EEU-5003	EEU-1529
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E

Caution The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

Documents Related to Development Tools (User's Manual) (2/2)

Document Name		Document No. Japanese	Document No. English
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	U10539E
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	U11279E

Documents Related to Embedded Software (User's Manual)

Document Name		Document No. Japanese	Document No. English
78K/0 Series OS MX78K0	Basic	U12257J	—
Fuzzy Knowledge Data Input Tools		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name	Document No. Japanese	Document No. English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	C11893J	MEI-1202
Microcomputer Product Series Guide	U11416J	—

Caution The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
NEC devices are classified into the following three quality grades:
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

- Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.
Anti-radioactive design is not implemented in this product.

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